IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 1-13, and AMEND claim 15 in accordance with the following:

1-13. (cancelled)

14. (original) An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction, said apparatus comprising:

a break detection section for detecting a breakpoint set at an arbitrary position of an instruction sequence;

a condition determination section for determining whether or not a condition of said conditional instruction is satisfied; and

a control section for controlling a break-interrupt on the basis of a breakpoint detection result from said break detection section and a determination result from said condition determination section.

15. (currently amended) An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction, said apparatus comprising:

an instruction break detection section for detecting an instruction break in accordance with whether or not an instruction corresponding to an instruction address representing a breakpoint, which is set in a register, is read out, and outputting a detection signal representing a detection result;

a condition determination section for determining whether or not a condition of the ~~read-out~~ conditional instruction is satisfied, and outputting a determination signal representing a determination result; and

a logical operation section for performing an AND operation to said detection signal output from said instruction break detection section and said determination signal output from said condition determination section, and sending a break-interrupt notification in accordance with the AND~~and~~ operation result.

16. (original) An apparatus according to claim 15, wherein

said condition determination section is designed to determine whether or not an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether or not the condition is satisfied, and output the determination signal representing the result, and

when an instruction word corresponding to the instruction address representing said breakpoint is an unconditional instruction or a conditional instruction having an unsatisfied condition, said logical operation section does not send a break-interrupt notification, and when said instruction word is the conditional instruction having a satisfied condition, said logical operation section sends said break-interrupt notification.

17. (original) An apparatus according to claim 15, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied,

said condition determination section is designed to determine whether or not an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether or not the condition is satisfied, and output the determination signal representing the result, and

in said first mode, when an instruction word corresponding to the instruction address representing said breakpoint is an unconditional instruction or a conditional instruction having an unsatisfied condition, said logical operation section does not sends a break-interrupt notification, and when said instruction word is the conditional instruction having a satisfied condition, said logical operation section sends a break-interrupt notification, and in said second mode, when said instruction word is an instruction word corresponding to the instruction address representing said breakpoint, said logical operation section sends said break-interrupt notification.

18. (original) An apparatus according to claim 15, wherein

said condition determination section is designed to determine whether or not an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether or not the condition is satisfied, and output the determination signal representing the result, and

when an instruction word corresponding to the instruction address representing said breakpoint is a conditional instruction having an unsatisfied condition, said logical operation section does not send a break-interrupt notification, and when said instruction word is an unconditional instruction or the conditional instruction having a satisfied condition, said logical operation section sends said break-interrupt notification.

19. (original) An apparatus according to claim 15, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generating when said generation condition of said instruction break is satisfied,

said condition determination section is designed to determine whether or not an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether or not the condition is satisfied, and output the determination signal representing the result, and

in said first mode, when an instruction word corresponding to the instruction address representing said breakpoint is a conditional instruction having an unsatisfied condition, said logical operation section does not send a break-interrupt notification, and when said instruction word is an unconditional instruction or the conditional instruction having a satisfied condition, said logical operation section sends a break-interrupt notification, and in said second mode, when said instruction word is an instruction word corresponding to the instruction address representing said breakpoint, said logical operation section sends said break-interrupt notification.

20. (original) An apparatus according to claim 15, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction, a long instruction word processor for parallelly executing short instructions forming a long instruction word, and a parallel processor for parallelly executing at least one basic instruction forming a variable-length instruction word.

21. (original) An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction, said apparatus comprising:

an instruction break detection section for detecting an instruction break in accordance

with whether or not an instruction corresponding to an instruction address representing a breakpoint, which is set in a register, is read out, and sending a break-interrupt notification in accordance with a detection result; and

a control section for, in an interrupt handler activated in accordance with said break-interrupt notification supplied from said instruction break detection section, determining whether or not a condition of said conditional instruction is satisfied, and controlling break-interrupt processing in accordance with a determination result.

22. (original) An apparatus according to claim 21, wherein said control section determines, in said interrupt handler, whether or not an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said instruction break target is a conditional instruction having a satisfied condition, performs said break-interrupt processing.

23. (original) An apparatus according to claim 21, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether or not an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said instruction break target is a conditional instruction having a satisfied condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

24. (original) An apparatus according to claim 21, wherein said control section

determines, in said interrupt handler, whether or not an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether a condition of said conditional instruction is satisfied, when said instruction word as said instruction break target is a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having a satisfied condition, performs said break-interrupt processing.

25. (original) An apparatus according to claim 21, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether or not an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said instruction break target is a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having a satisfied condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

26. (original) An apparatus according to claim 21, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction, a long instruction word processor for parallelly executing short instructions forming a long instruction word, and a parallel processor for parallelly executing at least one basic instruction forming a variable-length instruction word.

27. (original) An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction, said apparatus comprising:

a software break detection section for detecting a software break in accordance with whether or not a breakpoint instruction replaced at an arbitrary position of an instruction

sequence is executed, and sending a break-interrupt notification in accordance with a detection result; and

a control section for, in an interrupt handler activated in accordance with said break-interrupt notification supplied from said software break detection section, determining whether or not a condition of said conditional instruction is satisfied, and controlling break-interrupt processing in accordance with a determination result.

28. (original) An apparatus according to claim 27, wherein said control section determines, in said interrupt handler, whether or not an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said software break target is an unconditional instruction or a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said

instruction word as said software break target is a conditional instruction having a satisfied condition,

performs said break-interrupt processing.

29. (original) An apparatus according to claim 27, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said software break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generating when said generation condition of said software break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether or not an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said software break target is an unconditional instruction or a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said software break target is a conditional instruction having a satisfied condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

30. (original) An apparatus according to claim 27, wherein

said control section determines, in said interrupt handler, whether or not an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said software break target is a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said software break target is an unconditional instruction or a conditional instruction having a satisfied condition, performs said break-interrupt processing.

31. (original) An apparatus according to claim 27, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said software break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generating when said generation condition of said software break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether or not an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional

instruction is satisfied, when said instruction word as said software break target is a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said software break target is an unconditional instruction or a conditional instruction having a satisfied condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

32. (original) An apparatus according to claim 27, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction, a long instruction word processor for parallelly executing short instructions forming a long instruction word, and a parallel processor for parallelly executing at least one basic instruction forming a variable-length instruction word.

33. (original) An interrupt control method for controlling a break-interrupt in a data processing system having a function of executing a conditional instruction, said method comprising the steps of:

detecting a breakpoint set at an arbitrary position of an instruction sequence;

determining whether or not a condition of said conditional instruction is satisfied; and

controlling the break-interrupt on the basis of a detection result of said breakpoint and a determination result of said conditional instruction.